

**CLAIMS****What is claimed is:**

1. A multistage dynamic domino circuit comprising:  
a footed dynamic domino stage including:  
5           a first precharge circuit;  
            evaluation logic; and  
            a data output coupled to the evaluation logic;  
a footless dynamic domino stage including:  
            evaluation logic including a data input coupled to the data output of the footed  
10           dynamic domino stage; and  
            a second precharge circuit including:  
                a first precharge device including a first current terminal and a control  
                    terminal coupled to a clock line; and  
                a second precharge device including a first current terminal coupled to  
15           the first current terminal of first precharge device and a control  
                    terminal; and  
            a delay circuit including an input coupled to the clock line and an output  
                coupled to the control terminal of the second precharge device to provide  
                a delayed version of a clock signal provided at the input of the delay  
20           circuit.
2. The circuit of claim 1 wherein the first precharge circuit includes a P-channel device  
having control terminal coupled to the clock line.
3. The circuit of claim 1 wherein the delay circuit includes:  
a first inverter including an input coupled to the input of the delay circuit and an  
25           output; and  
a second input including an input coupled to the output of the first inverter and the  
output coupled to the output of the delay circuit.

4. The circuit of claim 1 wherein:  
the footed dynamic domino delay stage has a falling edge delay from a precharge  
edge of a clock signal provided to the precharge circuit of the footed dynamic  
domino stage to a falling edge of the data output; and
- 5 the delay circuit providing the delayed version with a delay of greater than the falling  
edge delay.
5. The circuit of claim 4 where the first precharge circuit is coupled to the clock line,  
wherein the clock signal is provided to the first precharge circuit via the clock line.
6. The circuit of claim 1 wherein:
- 10 the control terminal of the first precharge device is connected to the clock line;  
the input of the delay circuit is connected to the clock line; and  
the output of the delay circuit is connected to the control terminal of the second  
precharge device.
7. The circuit of claim 6 wherein the first precharge circuit of the footed dynamic
- 15 domino circuit includes a third precharge device including a control terminal, the control  
terminal of the third precharge device is connected to the clock line.
8. The circuit of claim 1 wherein during a precharge phase following an evaluation  
phase, the output of the delay circuit falls after a falling edge of the data output occurring  
during the precharge phase.
- 20 9. The circuit of claim 1 wherein entering an evaluation phase, the control terminal of  
the first precharge device receives a rising edge prior to a rising edge of the data out during  
the evaluation phase.
10. The circuit of claim 1 further comprising:
- 25 a second footless dynamic domino stage including:  
evaluation logic including a data input coupled to a data output of the footed  
dynamic domino stage; and  
a third precharge circuit including:

a third precharge device including a first current terminal and a control terminal coupled to the clock line; and  
 a fourth precharge device having a first current terminal coupled to the first current terminal of third precharge device and a control terminal; and  
 5 a second delay circuit including an input coupled to the clock line and an output coupled to the control terminal of the fourth precharge device to provide a delayed version of a clock signal provided to the input of the second delay circuit.

11. The circuit of claim 10 wherein the input of the second delay circuit is coupled to the  
 10 clock line via the delay circuit.

12. The circuit of claim 11 wherein the output of the second delay circuit provides a delayed version of the delay version of the clock signal provided at the input of the delay circuit.

13. The circuit of claim 10 wherein during a precharge phase following an evaluation  
 15 phase, the output of the second delay circuit falls after a falling edge of the data output of the footless dynamic domino stage occurring during the precharge phase.

14. The circuit of claim 10 wherein:  
 the first precharge device includes a first P-channel device;  
 the second precharge device includes a second P-channel device;  
 20 the third precharge device includes a third P-channel device;  
 the fourth precharge device includes a fourth P-channel device.

15. The circuit of claim 1 wherein the delay circuit and the footless dynamic domino stage are implemented in a single custom block of an integrated circuit.

16. The circuit of claim 1 wherein:  
 25 the first precharge device includes a first P-channel device;  
 the second precharge device includes a second P-channel device.

17. An integrated circuit including the multistage dynamic domino circuit of claim 1.

18. The integrated circuit of claim 17 further comprising:  
a processor, wherein the processor includes the multistage dynamic domino circuit.
19. A method of operating a multistage dynamic domino circuit, the method comprising:  
making non conductive a first precharge device of a footed dynamic domino stage to  
5 enter an evaluation phase, wherein the first precharge device is located in a first  
current path between evaluation logic of the footed dynamic domino stage and a  
voltage supply;  
making non conductive a second precharge device of a footless dynamic domino stage  
concurrently with the making non conductive the first precharge device, wherein  
10 the second precharge device is located in a second current path between  
evaluation logic of the footless dynamic domino stage and a voltage supply,  
wherein the evaluation logic of the footed dynamic domino stage is coupled to  
the evaluation logic of the footless dynamic domino stage;  
making conductive the first precharge device after the making non conductive non  
15 conductive the first precharge device to enter a precharge phase after the  
evaluation phase, wherein the making the first precharge device conductive  
makes conductive the first current path between the evaluation logic and the  
voltage supply;  
making conductive the second precharge device concurrently with the making  
20 conductive the first precharge device;  
making conductive a third precharge device located in the second current path after  
the making conductive the second precharge device, wherein the making  
conductive the third precharge device makes conductive the second current path  
between the evaluation logic of the footless dynamic domino stage and the  
25 voltage supply.
20. The method of claim 19 wherein:  
the first precharge device and the second precharge device each include a control  
terminal coupled to a clock line, wherein the making non conductive the first  
precharge device and the making non conductive the second precharge device  
30 include transitioning a clock signal provided on the clock line from a first state  
to a second state,

the making conductive the first precharge device and the making conductive the second precharge device include transitioning the clock signal from the second state to the first state;

the method further comprises delaying the clock signal to produce a delayed clock signal and providing the delayed clock signal to a control terminal of the third precharge device.

21. The method of claim 19 further comprising:

making non conductive a fourth precharge device of a second footless dynamic domino stage concurrently with the making non conductive the first precharge device, wherein the fourth precharge device is located in a third current path between evaluation logic of the second footless dynamic domino stage and a voltage supply, wherein the evaluation logic of the footless dynamic domino stage is coupled to evaluation logic of the second footless dynamic domino stage;

making conductive a fifth precharge device located in the third current path after the making conductive the fourth precharge device, wherein the making conductive the fifth precharge device makes conductive the third current path between the evaluation logic of the second footless dynamic domino stage and the voltage supply.

22. The method of claim 21 wherein the making conductive the fifth precharge device occurs during a precharge phase following an evaluation phase after a falling edge of a data output of the footless dynamic domino stage occurring during the precharge phase, the data output of the footless dynamic domino stage is coupled to the evaluation logic of the second footless dynamic domino stage.

23. The method of claim 19 wherein the making conductive the third precharge device occurs during a precharge phase following an evaluation phase after a falling edge of a data output of the footed dynamic domino stage occurring during the precharge phase, the data output of the footed dynamic domino stage is coupled to the evaluation logic of the footless dynamic domino stage.

24. The method of claim 19 wherein:  
the first precharge device includes a first P-channel device;  
the second precharge device includes a second P-channel device;  
the third precharge device includes a third P-channel device.

- 5 25. A multistage dynamic domino circuit comprising:  
a footed dynamic domino stage including:  
a first precharge circuit including a P-channel device, the P-channel device  
including a control terminal coupled to a clock line;  
evaluation logic including at least one N-channel device; and  
10 a data output coupled to the evaluation logic;  
a footless dynamic domino stage including:  
evaluation logic including a data input coupled to the data output of the footed  
dynamic domino stage, the evaluation logic including at least one N-  
channel device; and  
15 a second precharge circuit including:  
a second P-channel device including a first current terminal and a control  
terminal coupled to the clock line; and  
a third P-channel device having a first current terminal coupled to the first  
current terminal of second P-channel device and a control terminal; and  
20 a delay circuit including an input coupled to the clock line and an output  
coupled to the control terminal of the third P-channel device to provide a  
delayed version of a clock signal provided on the clock line.